Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (currently amended) A method for forming ~~on a silicon substrate~~ a non-volatile memory cell transistor in an array region ~~and a transistor in a region peripheral to the array region~~, the method comprising:

forming a ~~polysilicon~~ gate stack of the memory cell transistor in the array region~~, and a transistor polysilicon gate in the peripheral region~~;

forming ~~one of LDD and DDD regions in one or both~~ source and drain regions of the ~~transistor~~ memory cell transistor;

forming a spacer along one or more side-walls of ~~each of~~ the ~~cell~~ gate stack ~~and the transistor gate~~;

~~forming an oxide layer over the spacers, the cell gate stack, and the transistor gate;~~

~~forming a highly doped region in each of said one of the LDD and DDD regions, wherein a lateral distance between an outer edge of the highly doped diffusion region and an outer edge of a corresponding one of LDD and DDD regions is dependent at least on a thickness of the oxide layer;~~

defining a contact hole area over one or both of the drain and source regions of the memory cell transistor using a masking layer, wherein the contact hole area substantially abuts or overlaps the ~~polysilicon~~ gate stack; and

performing a contact etch to form a contact hole in the contact hole area, wherein ~~the spacer is substantially resistant to the contact etch~~ at least a portion of the spacer is not removed during the contact etch to provide insulation to the side-walls of the gate stack.

Claim 2 (currently amended) The method of claim 1 further comprising:

~~before the oxide layer forming act,~~ forming a sacrificial layer over the spacers, the cell gate stack, and the transistor gate.

Claim 3 (original) The method of claim 2 wherein the spacer and the sacrificial layer comprise nitride.

Claim 4 (currently amended) The method of claim 2 wherein the contact etch removes ~~the oxide layer and~~ part or all of the sacrificial layer.

Claim 5 (currently amended) The method of claim 1 ~~wherein the one of~~ further comprising:

forming one of LDD and DDD regions ~~forming act is carried out~~ in the memory cell transistor after the spacer ~~forming act but before the oxide layer forming act~~ is formed.

Claim 6 (original) The method of claim 1 wherein the spacer is insulated from the side-walls of polysilicon layers in the gate stack.

Claim 7 (original) The method of claim 1 further comprising:

forming an HTO layer over the gate stack ~~to insulate the gate stack from the spacer~~.

Claim 8 (currently amended) The method of claim 7 ~~further comprising:~~

~~forming~~ wherein the source and drain regions of the memory cell are formed after the HTO layer forming act.

Claim 9 (currently amended) The method of claim ~~1~~ 5 further comprising:

forming an oxide layer over the spacers and the gate stack;

~~prior to the highly doped region forming act,~~ performing an oxide etch to remove at least portions of the oxide layer over the drain and source regions of the transistor; and

forming a highly doped region in one of the LDD or DDD regions, wherein a lateral distance between an outer edge of the highly doped diffusion region and an outer edge of

a corresponding one of the LDD and DDD regions is dependent at least on a thickness of the oxide layer.

Claim 10 (original) The method of claim 1 further comprising:

prior to the spacer forming act, forming a DDD region in the source or drain region of the cell; and

after the spacer forming act, forming a highly doped region in the DDD region.

Claim 11 (original) The method of claim 1 wherein the memory cell is one of a split-gate cell and an ETOX stacked-gate cell.

Claims 12-17 (canceled)

Claim 18 (currently amended) A method for forming a non-volatile memory cell transistor in a memory array ~~and a transistor in a region peripheral to the memory array~~, the method comprising:

forming a plurality of gate layers on a semiconductor region;

forming first spacers adjacent to the gate layers in the memory array ~~and the transistor in the peripheral region~~;

~~forming an oxide film over the first spacers;~~

~~forming drain and source diffusion regions in the peripheral transistor;~~

~~masking and etching the oxide film~~ exposing the first spacers to a contact hole etch to form a contact hole to a drain or source region of the memory array transistor, wherein at least a portion of each of the first spacers ~~are substantially resistant to~~ is not removed during the contact hole etch; and

depositing a conductive layer on the memory cell transistor to form a contact to the drain or source region of the memory cell transistor, wherein the contact does not electrically connect to the gate layers of the memory cell transistor.

Claim 19 (currently amended) The method of claim 18 further comprising:

depositing a high thermal oxide film over the gate layers before the deposition of the first ~~etch-resistant~~ spacers.

Claim 20 (currently amended) The method of claim 18 further comprising:

forming an oxide film over the first spacers; and

etching the oxide film ~~prior to forming said drain and source diffusion regions in the peripheral region transistors~~ to remove a portion of the oxide film adjacent to the semiconductor region.

Claim 21 (original) The method of claim 18 wherein the first spacers are formed by depositing and etching a nitride layer, wherein the nitride layer is substantially resistant to the contact hole etch.

Claim 22 (original) The method of claim 18 further comprising:

depositing a nitride layer over the first spacers, after forming the first spacers.

Claim 23 (original) The method of claim 22 wherein portions of the nitride film are removed during the contact hole etch.

Claim 24 (original) The method of claim 18 wherein the first spacers have a width between 100-700 angstroms.

Claim 25 (currently amended) The method of claim 18 further comprising:

forming a transistor in a region peripheral to the memory array; and

forming a low doped drain region in the peripheral transistor before forming the first spacers adjacent to the gate layers.

Claim 26 (currently amended) The method of claim 18 further comprising:

forming a transistor in a region peripheral to the memory array; and

forming a double doped drain region in the peripheral transistor before forming the first spacers adjacent to the gate layers.

Claim 27 (currently amended) The method of claim 18 wherein a transistor is formed in a region peripheral to the memory array and ~~said~~ drain and source diffusion regions in the peripheral transistor are formed by depositing a first concentration of dopants within second drain and source diffusion regions in the peripheral transistor that are doped with a second concentration of dopants lower than the first concentration of dopants.

Claim 28 (currently amended) A method for forming a device comprising a plurality of transistors in a flash memory array ~~and a plurality of transistors in a peripheral region~~, the method comprising:

forming a plurality of gate layers on a semiconductor region;

forming first spacers adjacent to the gate layers of the transistors in the flash memory array ~~and the transistors in the peripheral region~~;

~~depositing a second film over the first spacers;~~

~~depositing an oxide film over the second film;~~

~~forming drain and source diffusion regions in the peripheral region transistors;~~

forming a contact mask over the plurality of gate layers that is aligned with edges of the gate layers; and

~~masking and etching the oxide film~~ performing a contact hole etch to form contact holes to drain or source regions of the memory array transistors,

wherein at least a portion of the first spacers ~~and the second film are substantially resistant to the contact hole etch, and the first spacers~~ are not removed during the contact hole etch such that the first spacers insulate lateral walls of the gate layers in the memory array transistors subsequent to the contact hole etch.

Claim 29 (original) The method of claim 28 further comprising:

depositing a high thermal oxide film over the gate layers before the formation of the first spacers.

Claim 30 (currently amended) The method of claim 28 further comprising:

depositing a second film over the first spacers;

depositing an oxide film over the second film;

forming drain and source diffusion regions in transistors located in a peripheral region of the device; and

etching the oxide film prior to forming said drain and source diffusion regions in the peripheral region transistors to remove a portion of the oxide film adjacent to the semiconductor region.

Claim 31(original) The method of claim 28 wherein the first spacers are formed by depositing and etching a nitride layer, wherein the nitride layer is substantially resistant to the contact hole etch.

Claim 32 (currently amended) The method of claim ~~28~~ 30 wherein the second film is formed by depositing a nitride layer.

Claim 33 (currently amended) The method of claim 32 wherein portions of the second film are removed during the contact hole etch.

Claim 34 (original) The method of claim 28 wherein the first spacers are between 100-700 angstroms wide.

Claim 35 (currently amended) A method for forming a non-volatile memory cell transistor in a memory array and a transistor in a region peripheral to the memory array, the method comprising:

forming a plurality of gate layers on a semiconductor region;

forming first spacers adjacent to the gate layers of the memory cell transistor and the transistor in the peripheral region;

~~depositing a second film over the first spacers;~~

~~depositing a first oxide film over the second film;~~

~~forming first drain and source diffusion regions in the peripheral region transistor;~~

~~depositing a second oxide film over the first oxide film;~~

~~forming second drain and source diffusion regions the peripheral region transistor;~~

and

masking and etching ~~the first and second oxide films~~ the gate layers to form contact holes to drain or source regions of the peripheral and memory array transistors,

wherein the first spacers ~~and the second film~~ are substantially resistant to the contact hole etch, and the first spacers insulate lateral walls of the gate layers in the memory array transistors and the peripheral region transistors subsequent to the contact hole etch.

Claim 36 (new) The method defined in claim 35 further comprising:

depositing a second film over the first spacers;

depositing a first oxide film over the second film;

forming first drain and source diffusion regions in the peripheral region transistor;

depositing a second oxide film over the first oxide film; and

forming second drain and source diffusion regions the peripheral region transistor.